

## CLAIMS

What is claimed:

5      1. A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:

10      providing a semiconductor substrate having a Cu surface formed in a via;

15      providing a chemical solution;

20      electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;

25      rinsing the Cu-Zn alloy fill in a solvent;

30      drying the Cu-Zn alloy fill under a gaseous flow;

35      annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming a reduced-oxygen Cu-Zn alloy fill;

40      planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and

45      completing formation of the semiconductor device.

5      2. A method, as recited in Claim 1,  
wherein the chemical solution is nontoxic and aqueous, and  
wherein the chemical solution comprises:  
at least one zinc (Zn) ion source for providing a plurality of Zn ions;  
at least one copper (Cu) ion source for providing a plurality of Cu ions;  
at least one complexing agent for complexing the plurality of Cu ions;  
at least one pH adjuster;  
at least one wetting agent for stabilizing the chemical solution, all being dissolved in a volume of deionized (DI) water.

3. A method, as recited in Claim 2,  
 wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected  
 from a group consisting essentially of zinc acetate ((CH<sub>3</sub>CO<sub>2</sub>)<sub>2</sub>Zn), zinc  
 bromide (ZnBr<sub>2</sub>), zinc carbonate hydroxide (ZnCO<sub>3</sub>·2Zn(OH)<sub>2</sub>), zinc  
 5 dichloride (ZnCl<sub>2</sub>), zinc citrate ((O<sub>2</sub>CCH<sub>2</sub>C(OH)(CO<sub>2</sub>)CH<sub>2</sub>CO<sub>2</sub>)<sub>2</sub>Zn<sub>3</sub>), zinc  
 iodide (ZnI<sub>2</sub>), zinc L-lactate ((CH<sub>3</sub>CH(OH)CO<sub>2</sub>)<sub>2</sub>Zn), zinc nitrate (Zn(NO<sub>3</sub>)<sub>2</sub>),  
 zinc stearate ((CH<sub>3</sub>(CH<sub>2</sub>)<sub>16</sub>CO<sub>2</sub>)<sub>2</sub>Zn), zinc sulfate (ZnSO<sub>4</sub>), zinc sulfide (ZnS),  
 zinc sulfite (ZnSO<sub>3</sub>), and their hydrates.

4. A method, as recited in Claim 2,  
 wherein the at least one copper (Cu) ion source comprises at least one copper salt  
 selected from a group consisting essentially of copper(I) acetate  
 (CH<sub>3</sub>CO<sub>2</sub>Cu), copper(II) acetate ((CH<sub>3</sub>CO<sub>2</sub>)<sub>2</sub>Cu), copper(I) bromide (CuBr),  
 5 copper(II) bromide (CuBr<sub>2</sub>), copper(II) hydroxide (Cu(OH)<sub>2</sub>), copper(II)  
 hydroxide phosphate (Cu<sub>2</sub>(OH)PO<sub>4</sub>), copper(I) iodide (CuI), copper(II)  
 nitrate ((CuNO<sub>3</sub>)<sub>2</sub>), copper(II) sulfate (CuSO<sub>4</sub>), copper(I) sulfide (Cu<sub>2</sub>S),  
 copper(II) sulfide (CuS), copper(II) tartrate ((CH(OH)CO<sub>2</sub>)<sub>2</sub>Cu), and their  
 hydrates.

5. A method, as recited in Claim 1,  
 wherein said electroplating step comprises using an electroplating apparatus, and  
 wherein said electroplating apparatus comprises:  
 (a) a cathode-wafer;  
 (b) an anode;  
 (c) an electroplating vessel; and  
 (d) a voltage source.

6. A method, as recited in Claim 5,  
 wherein the cathode-wafer comprises the Cu surface, and  
 wherein the anode comprises at least one material selected from a group consisting  
 essentially of copper (Cu), a copper-platinum alloy (Cu-Pt), titanium (Ti),  
 platinum (Pt), a titanium-platinum alloy (Ti-Pt), an anodized copper-zinc  
 5 alloy (Cu-Zn, i.e., brass), a platinized titanium (Pt/Ti), and a platinized  
 copper-zinc (Pt/Cu-Zn, i.e., platinized brass).

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7. A method, as recited in Claim 1,  
wherein said semiconductor substrate further comprises a barrier layer formed in the  
via under said Cu surface, and  
wherein the barrier layer comprises at least one material selected from a group  
5 consisting essentially of titanium silicon nitride ( $Ti_xSi_yN_z$ ), tantalum nitride  
(TaN), and tungsten nitride ( $W_xN_y$ ).

8. A method, as recited in Claim 7,  
wherein said semiconductor substrate further comprises an underlayer formed on the  
barrier layer,  
wherein said underlayer comprises at least one material selected from a group  
5 consisting essentially of tin (Sn) and palladium (Pd), and  
wherein said Cu surface is formed over said barrier layer and on said underlayer.

9. A method, as recited in Claim 8,  
wherein said underlayer comprises a thickness range of approximately 15 Å to  
approximately 50 Å,  
wherein said barrier layer comprises a thickness range of approximately 30 Å to  
approximately 50 Å,  
wherein said Cu surface comprises a thickness range of approximately 50 Å to  
approximately 70 Å, and  
wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to  
approximately 700 Å.

10. A method, as recited in Claim 1,  
wherein the annealing steps are performed in a temperature range of approximately  
150°C to approximately 450°C, and  
5 wherein the annealing steps are performed for a duration range of approximately 0.5  
minutes to approximately 60 minutes.

11. A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:

providing a semiconductor substrate having a Cu surface formed in a via;

providing a chemical solution;

electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy

fill in the via and on the Cu surface;

rinsing the Cu-Zn alloy fill in a solvent;

10 drying the Cu-Zn alloy fill under a gaseous flow;  
annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming

a reduced-oxygen Cu-Zn alloy fill;

planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing  
formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect  
structure; and

completing formation of the semiconductor device.

12. A device, as recited in Claim 11,

wherein the chemical solution is nontoxic and aqueous, and

wherein the chemical solution comprises:

at least one zinc (Zn) ion source for providing a plurality of Zn ions;

5 at least one copper (Cu) ion source for providing a plurality of Cu ions;

at least one complexing agent for complexing the plurality of Cu ions;

at least one pH adjuster;

at least one wetting agent for stabilizing the chemical solution, all being  
dissolved in a volume of deionized (DI) water.

13. A device, as recited in Claim 12,

wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected  
from a group consisting essentially of zinc acetate  $((\text{CH}_3\text{CO}_2)_2\text{Zn})$ , zinc  
bromide  $(\text{ZnBr}_2)$ , zinc carbonate hydroxide  $(\text{ZnCO}_3 \cdot 2\text{Zn}(\text{OH})_2)$ , zinc  
5 dichloride  $(\text{ZnCl}_2)$ , zinc citrate  $(\text{O}_2\text{CCH}_2\text{C}(\text{OH})(\text{CO}_2)\text{CH}_2\text{CO}_2)_2\text{Zn}_3$ , zinc

iodide ( $ZnI_2$ ), zinc L-lactate ( $(CH_3CH(OH)CO_2)_2Zn$ ), zinc nitrate ( $Zn(NO_3)_2$ ), zinc stearate ( $(CH_3(CH_2)_{16}CO_2)_2Zn$ ), zinc sulfate ( $ZnSO_4$ ), zinc sulfide ( $ZnS$ ), zinc sulfite ( $ZnSO_3$ ), and their hydrates.

14. A device, as recited in Claim 12,

wherein the at least one copper (Cu) ion source comprises at least one copper salt selected from a group consisting essentially of copper(I) acetate ( $CH_3CO_2Cu$ ), copper(II) acetate ( $(CH_3CO_2)_2Cu$ ), copper(I) bromide ( $CuBr$ ), copper(II) bromide ( $CuBr_2$ ), copper(II) hydroxide ( $Cu(OH)_2$ ), copper(II) hydroxide phosphate ( $Cu_2(OH)PO_4$ ), copper(I) iodide ( $CuI$ ), copper(II) nitrate hydrate ( $(CuNO_3)_2$ ), copper(II) sulfate ( $CuSO_4$ ), copper(I) sulfide ( $Cu_2S$ ), copper(II) sulfide ( $CuS$ ), copper(II) tartrate ( $(CH(OH)CO_2)_2Cu$ ), and their hydrates.

15. A device, as recited in Claim 11,

wherein said electroplating step comprises using an electroplating apparatus, and wherein said electroplating apparatus comprises:

- (a) a cathode-wafer;
- (b) an anode;
- (c) an electroplating vessel; and
- (d) a voltage source.

16. A device, as recited in Claim 15,

wherein the cathode-wafer comprises the Cu surface, and

wherein the anode comprises at least one material selected from a group consisting essentially of copper (Cu), a copper-platinum alloy (Cu-Pt), titanium (Ti), platinum (Pt), a titanium-platinum alloy (Ti-Pt), an anodized copper-zinc alloy (Cu-Zn, i.e., brass), a platinized titanium (Pt/Ti), and a platinized copper-zinc (Pt/Cu-Zn, i.e., platinized brass).

17. A device, as recited in Claim 11,  
wherein said semiconductor substrate further comprises a barrier layer formed in the  
via under said Cu surface, and  
wherein the barrier layer comprises at least one material selected from a group  
5 consisting essentially of titanium silicon nitride ( $Ti_xSi_yN_z$ ), tantalum nitride  
(TaN), and tungsten nitride ( $W_xN_y$ )

18. A device, as recited in Claim 17,  
wherein said semiconductor substrate further comprises an underlayer formed on the  
barrier layer,  
wherein said underlayer comprises at least one material selected from a group  
5 consisting essentially of tin (Sn) and palladium (Pd), and  
wherein said Cu surface is formed over said barrier layer and on said underlayer.

19. A device, as recited in Claim 18,  
wherein said underlayer comprises a thickness range of approximately 15 Å to  
approximately 50 Å,  
wherein said barrier layer comprises a thickness range of approximately 30 Å to  
50 Å,  
wherein said Cu surface comprises a thickness range of approximately 50 Å to  
approximately 70 Å, and  
wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to  
approximately 700 Å.

20. A semiconductor device, having a first interim reduced-oxygen copper-zinc (Cu-Zn)  
alloy fill formed on a copper (Cu) surface and a second interim reduced-oxygen Cu-  
Zn alloy fill formed on a Cu-fill, both films being formed by electroplating the Cu  
surface and the Cu-fill, respectively, in a chemical solution, comprising:  
5 a semiconductor substrate having a via; and  
an encapsulated dual-inlaid interconnect structure formed and disposed in said via,  
said interconnect structure comprising:  
at least one Cu surface formed in said via;

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- a first interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the at least one Cu surface;
- a Cu-fill formed and disposed on said interim reduced-oxygen Cu-Zn alloy fill; and
- a second interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the Cu-fill.